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PATENT APPLICATION

IMAGE REJECT CIRCUIT USING SIGMA-DELTA CONVERSION

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CROSS-REFERENCES TO RELATED APPLICATIONS

[01] NOT APPLICABLE

STATEMENT AS TO RIGHTS TO INVENTIONS MADE UNDER FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

[02] NOT APPLICABLE

REFERENCE TO A "SEQUENCE LISTING," A TABLE, OR A COMPUTER PROGRAM LISTING APPENDIX SUBMITTED ON A COMPACT DISK.

[03] NOT APPLICABLE

BACKGROUND OF THE INVENTION

[04] This invention relates to digital IF downconversion and particularly to digital IF downconversion of relatively wide bandwidth signals at microwave frequencies.

[05] Digital IF downconversion has the advantage of flexibility for multi-mode operation, such as is useful for multiple modes of cellular communication and controllable accuracy and thus good performance with wide bandwidth signals wherever the sampling rate and coefficient accuracy is adequate for the frequencies of interest. In typical operation, the full bandwidth range is captured in an analog-to-digital converter employing a bandpass sigma-delta converter, followed by a final digital filtering channel.

[06] The challenge of processing a wideband digital IF converted signal is rejection of unwanted image and spurious signals which when they occur on the frequency of interest block the desired signal (and hence are called blockers). For this purpose, a DSP filter that is programmed for the appropriate mode of operation is commonly used following wideband downconversion.

[07] Figure 1 illustrates one typical configuration of a downconverter circuit 100 with an image reject stage. Radio Frequency (RF) signals are processed through an in-phase (I) channel 102 and a quadrature phase channel 104 implemented by downconverting mixers 106 and 108 referenced to an analog reference signal of an analog source 110, wherein the reference signals are precisely 90 degrees out of phase (as represented by a 90 degree or $\pi/2$

delay element 112). The reference signal has a typical operating frequency of 100 kHz below the nominal RF frequency. The analog signals are processed through conventional sigma-delta analog to digital converters 114, 116 to produce respective one-bit wide serial bit streams. Each channel of the circuit 100 includes a decimator 118, 120 to convert the high-speed serial bit streams to parallel bit streams. There are typically four or eight parallel streams in each path. The parallel bit streams are each supplied to respective fractional filters to make the sampling integer in nature. There is a corresponding compensation filter function for extracting the desired signal of the defined bandwidth. These two functions may be combined in a digital finite impulse response (FIR) filter 122, 124 whose characteristics are defined by a set of filter coefficients.

[08] It is known that out-of-bandwidth attenuation degrades as fewer bits are used to represent filter coefficients. Thus, overall performance depends on the number of bits employed to represent the filter characteristic. The outputs of the FIR filters 122, 124 are mixed and summed digitally in a mixing/summing stage 126 to cancel the unwanted components and to generate as output I and Q multi-bit digital bit streams representing the pure I component and the pure Q component of the wanted signal with maximum image rejection. The digital I and Q components are then processed through digital-to-analog converters 128, 130 (operating at the Nyquist rate) to recover the signal as I and Q analog components 132, 134 at baseband.

[09] This conventional image cancellation scheme has a number of practical drawbacks. According to the conventional approach, in order to achieve targeted performance levels, it has been a practice to use relatively power-consumptive parallel processing techniques operative on the in-phase and quadrature signal components in the form of digital word streams. Not only do these techniques consume more power than is desirable, they also require deployment of relatively large integrated circuits. In a typical configuration, the decimators 118, 120, FIR filter 122, 124, the summing stage 126 and the DACs 128, 130 require on the order of 25,000 gates to implement, which translates to almost 3 square millimeters of valuable circuit area and relatively high power consumption. Both power and circuit size are premium in a portable battery operated digital device such as a cellular telephone.

[10] A representative description of one published prior art implementation is Rudell et al., "A 1.9 GHz Wide-Band IF Double Conversion CMOS Receiver for Cordless Telephone Applications," *IEEE Journal of Solid-State Circuits*, Vol. 32, No. 12, December 1997.

[11] Another representative reference is Canadian patent application 2,284,948 published April 4, 2001 of Birkett et al.

[12] What is needed is a more efficient image reject circuit in a digital IF downconversion circuit for a portable digital device such as a cellular telephone.

SUMMARY OF THE INVENTION

[13] According to the invention, in a digital IF downconversion circuit, in-phase and quadrature signal components are processed in the form of a parallel channels of single serial digital bit stream through a set of simple logic elements, such as a novel grouping of Exclusive OR gates, AND gates and OR gates, operating as adders and multipliers in combination with a "reconstruction filter" to recover the analog in-phase and quadrature phase baseband components substantially free of images. In a preferred embodiment, the two bit streams output from I and Q sigma-delta A/D converter are split and then each exclusive-ORed with both a high accuracy sine function and a cosine function bit stream, then the outputs of the XOR gates are each both ORed together and ANDed together. This Boolean product and this Boolean sum are then each binary weighted and combined in a reconstruction filter formed of weighting resistors that are combined with other weighted outputs to form respective analog I and Q channel signals at baseband.

[14] Further specifically according to the invention, a source digital oscillator supplying digital signal mixers employs an oversampled digital word of four bits in length, all of which are binary weighted relative to one another, to achieve at least sixteen levels of accuracy for a sine wave mixing signal without significant phase or amplitude error. The mixer mixes the digitized serial bit stream according to the clock with output of a four-bit wide digital cosine/sine table representing the source oscillator by means of a simple exclusive OR, and the in-phase and quadrature signals are recombined digitally using a simple AND and OR summer, followed by binary weighting using weighted resistors coupled into a filter. Thus, image rejection is a digital function which is unaffected by resistor tolerance.

The invention will be better understood by reference to the following detailed description in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[15] Figure 1 is a block diagram of a prior art digital RF downconverter.

[16] Figure 2 is a block diagram of a digital RF down converter according to the invention.

[17] Figure 3 is a block diagram of a cosine/sine generator suitable for use according to the invention.

DETAILED DESCRIPTION OF THE INVENTION

[18] Referring to Figure 2, a sigma delta low IF image reject circuit 200 according to the invention is shown. Not shown is the front end of the receiver, which typically comprises a surface acoustic wave (SAW) filter and low noise amplifier (LNA) which feed RF signals to an input splitter 201. The outputs from the splitter 201 provide the source for first and second quadrature low side injection mixers 206, 208, which are driven by a first local oscillator 210 at a frequency of LO = RF-100kHz. The 100kHz signal is selected to conform with the channel spacing requirements. A linear 90 degree phase shifter 212 assures a constant quadrature relation between the signals. As a consequence, where the local oscillator 210 is referenced to an analog cosine signal, the output of the first mixer 206 is of the frequencies:

[19] -sin(RF-LO); and

[20] -sin(RF+LO).

[21] The output of the second mixer 208 is of the frequencies:

[22] cos(RF-LO); and

[23] cos(RF+LO).

[24] This means that both the wanted signal and the image mix down to 100kHz. The outputs of the mixers 206, 208 each then feed into first and second low-pass filters 202, 203 to reject the respective signals -sin(RF+LO) and cos(RF+LO).

[25] After the filter 202, 203, the signals -sin(RF-LO) and cos(RF-LO) are fed to respective sigma-delta analog to digital converters 214, 216 to produce a single serial bit stream output. For the purposes of illustration only, the output is shown as two pairs of four parallel channels as hereinafter explained so they can interact with corresponding bits of sine and cosine tables 219, 221 over-clocked by a 39MHz clock/counter 222. The clocked tables together define an effective second local oscillator to mix down the 100kHz signal to baseband while rejecting the image. For purposes of explanation, the outputs of the sigma-delta converters 214, 216 are shown as four parallel lines each A, B, C, D and A', B', C' and D' corresponding to the Most Significant Bit to Least Significant Bit associated with the converter outputs. The bits are actually fed serially on a common line. These bits are synchronized to the bits supplied from the cosine table 219 and the sine table 221 by appropriate timing. The complete sine table and cosine for sixteen levels over one-quarter cycle is reproduced below in connection with the circuit of Figure 3. These values are stored in memory locations or elements, as hereinafter explained.

[26] Table Loc. SineTable Cosine Table

[27] _____

	[28]	1	1	0	0	0	1	1	1	1
	[29]	2	1	0	0	0	1	1	1	1
	[30]	3	1	0	0	0	1	1	1	1
	[31]	4	1	0	0	0	1	1	1	1
5	[32]	5	1	0	0	0	1	1	1	1
	[33]	6	1	0	0	0	1	1	1	1
	[34]	7	1	0	0	1	1	1	1	1
	[35]	8	1	0	0	0	1	1	1	1
	[36]	9	1	0	0	1	1	1	1	1
10	[37]	10	1	0	0	0	1	1	1	1
	[38]	11	1	0	0	1	1	1	1	1
	[39]	12	1	0	0	1	1	1	1	1
	[40]	13	1	0	0	1	1	1	1	1
	[41]	14	1	0	1	0	1	1	1	1
15	[42]	15	1	0	0	1	1	1	1	1
	[43]	16	1	0	0	1	1	1	1	1
	[44]	17	1	0	1	0	1	1	1	1
	[45]	18	1	0	1	0	1	1	1	1
	[46]	19	1	0	1	0	1	1	1	1
20	[47]	20	1	0	0	1	1	1	1	1
	[48]	21	1	0	1	1	1	1	1	1
	[49]	22	1	0	1	0	1	1	1	1
	[50]	23	1	0	1	0	1	1	1	1
	[51]	24	1	0	1	0	1	1	1	0
25	[52]	25	1	0	1	1	1	1	1	1
	[53]	26	1	0	1	0	1	1	1	0
	[54]	27	1	0	1	1	1	1	1	1
	[55]	28	1	0	1	1	1	1	1	0
	[56]	29	1	0	1	1	1	1	1	1
30	[57]	30	1	0	1	1	1	1	1	0
	[58]	31	1	0	1	1	1	1	1	0
	[59]	32	1	0	1	1	1	1	1	0
	[60]	33	1	1	0	0	1	1	1	0
	[61]	34	1	0	1	1	1	1	1	0

	[62]	35	1	1	0	0	1	1	1	0
	[63]	36	1	0	1	1	1	1	1	0
	[64]	37	1	1	0	0	1	1	1	0
	[65]	38	1	1	0	0	1	1	1	0
	[66]	39	1	1	0	0	1	1	0	1
	[67]	40	1	1	0	0	1	1	1	0
	[68]	41	1	1	0	0	1	1	0	1
	[69]	42	1	1	0	0	1	1	1	0
	[70]	43	1	1	0	1	1	1	0	1
	[71]	44	1	1	0	0	1	1	0	1
	[72]	45	1	1	0	1	1	1	0	1
	[73]	46	1	1	0	0	1	1	1	0
	[74]	47	1	1	0	1	1	1	0	1
	[75]	48	1	1	0	1	1	1	0	1
	[76]	49	1	1	0	0	1	1	0	0
	[77]	50	1	1	0	1	1	1	0	1
	[78]	51	1	1	0	1	1	1	0	1
	[79]	52	1	1	1	0	1	1	0	0
	[80]	53	1	1	0	1	1	1	0	1
	[81]	54	1	1	0	1	1	1	0	0
	[82]	55	1	1	0	1	1	1	0	1
	[83]	56	1	1	1	0	1	1	0	0
	[84]	57	1	1	0	1	1	1	0	0
	[85]	58	1	1	1	0	1	1	0	0
	[86]	59	1	1	0	1	1	1	0	0
	[87]	60	1	1	1	0	1	1	0	0
	[88]	61	1	1	1	0	1	1	0	0
	[89]	62	1	1	1	0	1	0	1	1
	[90]	63	1	1	1	0	1	1	0	0
	[91]	64	1	1	1	0	1	0	1	1
	[92]	65	1	1	1	0	1	1	0	0
	[93]	66	1	1	1	0	1	0	1	1
	[94]	67	1	1	1	0	1	0	1	1
	[95]	68	1	1	1	0	1	0	1	1

[96]	69	1	1	1	1	1	0	1	1
[97]	70	1	1	1	0	1	0	1	1
[98]	71	1	1	1	1	1	0	1	1
[99]	72	1	1	1	0	1	0	1	0
[100]	73	1	1	1	1	1	0	1	1
[101]	74	1	1	1	0	1	0	1	0
[102]	75	1	1	1	1	1	0	1	0
[103]	76	1	1	1	1	1	0	1	0
[104]	77	1	1	1	1	1	0	1	1
[105]	78	1	1	1	1	1	0	0	1
[106]	79	1	1	1	1	1	0	1	0
[107]	80	1	1	1	1	1	0	1	0
[108]	81	1	1	1	1	1	0	1	0
[109]	82	1	1	1	1	1	0	0	1
[110]	83	1	1	1	1	1	0	0	1
[111]	84	1	1	1	1	1	0	1	0
[112]	85	1	1	1	1	1	0	0	1
[113]	86	1	1	1	1	1	0	0	1
[114]	87	1	1	1	1	1	0	0	1
[115]	88	1	1	1	1	1	0	0	0
[116]	89	1	1	1	1	1	0	0	1
[117]	90	1	1	1	1	1	0	0	0
[118]	91	1	1	1	1	1	0	0	1
[119]	92	1	1	1	1	1	0	0	0
[120]	93	1	1	1	1	1	0	0	0
[121]	94	1	1	1	1	1	0	0	0
[122]	95	1	1	1	1	1	0	0	0
[123]	96	1	1	1	1	1	0	0	0
[124]	97	1	1	1	1	1	0	0	0
[125]	98	1	1	1	1	0	1	1	1

[126]

[127] The clock/counter 222 comprises a 39 MHz clock 612, an up/down binary counter 614 which outputs a seven-bit address word, and an up vs. down logic selector 616 which

reads the counter 614 output and reverses the count direction at peaks and at zero address positions.

[128] The sine table 221 comprises an addressable memory such as a ROM 602 containing the values of the sine table above and inversion logic 604 for converting the values according to the appropriate quadrants of the cycle. The cosine table comprises an addressable memory such as a ROM 606 containing the values of the cosine table above and inversion logic for converting the values according to the same quadrants. Inversion detector 610 is shared with the inversion logic elements 604, 608 and reads the output of counter 614 to sense zero crossing positions and add the appropriate sign bit.

[129] The two bit streams output from I and Q sigma-delta A/D converters 214, 216 are split and then each exclusive-ORed with both the corresponding sine function bits from sine table 221 and the cosine function bits from cosine table 219. Then the outputs of the XOR gates are each both ORed together and ANDed together. This Boolean product and this Boolean sum are then each binary weighted and combined in an reconstruction filter formed of weighting resistors that are combined with other weighted outputs to form respective analog I and Q channel signals at baseband.

[130] In a specific embodiment according to the invention, a bank of pairs of digital signal mixers 223, 225; 323, 325; 423, 425; 523, 525 are provided using for example XOR gates 229, 231 with an AND gate 235 and an OR gate 233 in one of the pair, and further using XOR gates 237, 239 with an AND gate 243 and an OR gate 241 in the other of the pair.

[131] The source digital oscillator supplying the digital signal mixers employs an oversampled digital word of four bits in length, all of which are binary weighted relative to one another, to achieve at least sixteen levels of accuracy for a sine wave mixing signal without significant phase or amplitude error. The mixer 223, 225 mixes the digitized serial bit stream from converters 214 and 216 according to the clock, at 39 MHz for example, with the output of the four-bit wide digital cosine/sine tables 219/221 representing the source oscillator by means of a simple exclusive-OR at gates 229, 231, and the in-phase and quadrature signals are recombined digitally using a simple AND and OR summer 233, 235. For the Most Significant Bit (MSB) of the In-phase channel, one bit output of the converter 214 is XORed with the corresponding sin bit in the first XOR gate 229 and is simultaneously XORed with the corresponding cos bit in the second XOR gate 231. The output of the first XOR gate 229 is ORed in the first OR gate 233 with the output of the second XOR gate 231, while the output of the first XOR gate 229 is simultaneously ANDed in the second AND gate

235 with the output of the second XOR gate 231. The result is the desired I channel signal ready for analog scaling according to the weighting of the bit.

[132] For the Most Significant Bit (MSB) of the Quadrature-phase channel, one bit output of the converter 216 is XORed with the corresponding cos bit in the third XOR gate 237 and is simultaneously XORed with the corresponding sin bit in the fourth XOR gate 239. The output of the third XOR gate 237 is ORed in the second OR gate 241 with the output of the fourth XOR gate 239, while the output of the third XOR gate 237 is simultaneously ANDed in the second AND gate 243 with the output of the fourth XOR gate 239. The result is the desired Q channel signal ready for analog scaling according to the weighting of the bit.

[133] This configuration and operation is performed for each significant bit output from the converters 214, 216, effectively operating in parallel.

[134] The output of the final gates are followed by binary weighting using weighting resistors of value R, 2R, 4R and 8R, corresponding to their respective binary values. Each channel is summed at a summing node 250, 252 coupled at respective capacitors 254, 256 serving as lowpass filters F1, F2. The resultant output is the analog I channel 258 with signal –cos(RF-LO-LO2) and Q channel 260 with signal –sin(RF-LO-LO2), both with desired image rejection.

[135] The image rejection is typcially limited by the tolerance of the weighting resistors. While initial image rejection is as high as –35dBc, once the first mixers have contributed their error, the image rejection is much less. It is thus better to do the summation digitally and then reconstruct the outputs into the filter afterwards. This method means that the image rejection is not affected by the resistor tolerance but only by the harmonic rejection of the sine and cosine table.

[136] In the GSM band plan, the channel spacing is 200kHz, which requires a quadrature second Local Oscillator frequency to be 100kHz. A square wave at 100kHz would mix down not only the wanted to baseband but all odd harmonics of the 100kHz passband. The third harmonic (300kHz) is the adjacent channel and the fifth harmonic (500kHz) is the bi-adjacent channel. Thus, all channels are mixed to some degree into the wanted passband. The use of highly-accurate (16 level) oversampled sine/cosine table overcomes much of this problem.

[137] The bandwidth of the reconstruction filters 254, 256 (Figure 2) are not critical because they merely need to provide rejection of the high frequency switching noise in the MHz region. The pole should be set so that it does not attenuate the maximum 67kHz deviation from the design bandwidth for GMSK but will provide maximum attenuation of all higher

frequencies. This type of filter can be implemented either as an R-C circuit as illustrated or as a charge pump circuit feeding an external capacitor (not shown).

[138] It has been found that even with blockers larger than allowed by the GSM 05:05 Specification they will not be mixed down to baseband to a degree where they will degrade performance. It has also been found that with –104dBm input to the low IF receiver board the LO2 level is –8dBc from the wanted. This is obtained without trying to correct for the sigma delta comparator DC bias level and offset voltage level. The image rejection has been measured at –17dBc with no correction for the front end amplitude/phase errors and while using RC components in the sigma delta whose bandwidth tolerance is unknown. In any event, the number of gates required to implement the circuit is reduced by an order of magnitude.

[139] The invention has been explained with reference to specific drawings and embodiments. Other embodiments will be evident to those of ordinary skill in the art. It is therefore intended that the invention not be limited except as indicated by the appended claims.